HighSNR Lab

Application Note AN-001

Frequency-Dependent Distortion in Class II Ceramic Capacitors

Why THD Peaks Near the RC Transition Band – and How Incorrect C(V) Simulation Creates False Harmonics

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ABSTRACT: Class II ceramic capacitors, including X7R and X5R MLCCs, exhibit voltage-dependent capacitance that can create measurable harmonic distortion in analog signal paths. This note shows why output-voltage THD in a first-order RC low-pass network can peak near the transition band, where capacitor voltage swing and circuit current are both significant. It also separates this physical effect from a simulation trap: numerical harmonics caused by updating a nonlinear capacitor from a locally frozen C(V) value instead of solving a charge-consistent Q(V) relation.

Revision History

Rev	Date	Change	Author
A	July 27, 2026	Public Release	B. Kuznetsov

1. Introduction and Scope

This application note analyzes a simple first-order RC low-pass network using a voltage-dependent Class II ceramic capacitor. The goal is not to provide a vendor-accurate MLCC macromodel. Instead, the goal is to isolate two engineering effects:

1. The physical distortion mechanism caused by voltage-dependent differential capacitance.
2. The numerical distortion mechanism caused by incorrect behavioral modeling of nonlinear capacitance.

The analysis is intended for analog designers, signal-chain engineers, and engineers building behavioral simulation models for nonlinear passive components.

2. Background: Voltage-Dependent Capacitance

Class II ceramic capacitors use high-permittivity dielectric materials. These materials provide high capacitance density, but their capacitance is not constant. The effective capacitance depends on DC bias, AC voltage swing, temperature, aging, dielectric formulation, package geometry, and frequency-dependent dielectric behavior [1], [4].

For small-signal linear analysis, a capacitor is often treated as:

$$i(t) = C\frac{dV(t)}{dt} \tag{1}$$

where C is constant.

For a nonlinear ceramic capacitor, the physically meaningful relation is instead charge-based:

$$i(t) = \frac{dQ(V)}{dt} \tag{2}$$

and the differential capacitance is:

$$C_{\text{diff}}(V) = \frac{dQ(V)}{dV} \tag{3}$$

This distinction is not cosmetic. It determines whether the simulated capacitor conserves charge.

A simplified empirical form for the differential capacitance may be written as:

$$C_{\text{diff}}(V) = \frac{C_0}{1 + kV^2} \tag{4}$$

where C_0 is the zero-bias capacitance; and k is a fitting parameter describing the strength of the voltage coefficient.

In this note, $C_{\text{diff}}(V)$ always means differential capacitance, not the large-signal ratio Q/V.

2.1. Real-component context

Figure 2 shows how strongly a real compact X5R part can depart from its zero-bias value. The curve is a Murata SimSurfing export for GRM155R60J105KE19 (1 μF, 6.3 V, X5R, 0402), identified in the export header

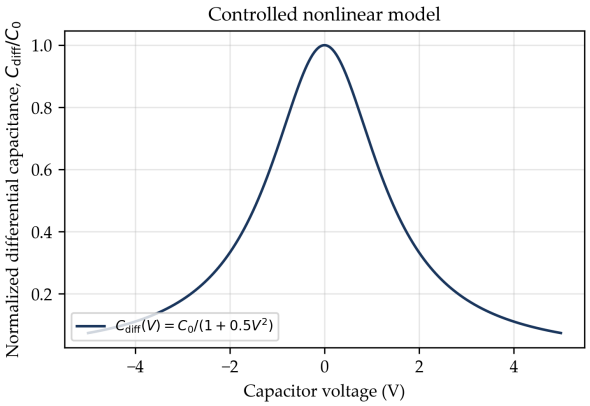

Figure 1: Controlled symmetric differential-capacitance model used in the main simulation. It is an illustrative test function, not data for a commercial capacitor. Parameters: $C_0 = 1\,\mu$F and $k = 0.5\,\mathrm{V}^{-2}$.

as 25 °C and 10 mV RMS [5], [6]. The export does not record test frequency, dwell time, sweep direction, or uncertainty. It is therefore used here only to demonstrate real bias curvature. It is not substituted into the controlled simulation and does not establish large-signal THD accuracy.

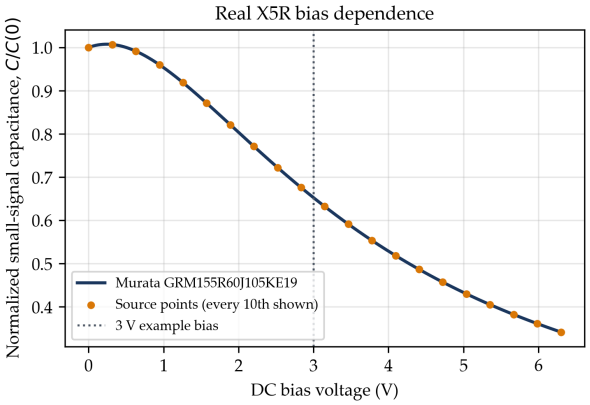

Figure 2: Normalized small-signal capacitance from a Murata SimSurfing export for GRM155R60J105KE19. Source-file SHA-256: `39d3babb...b48270`.

3. Test Circuit

Consider the first-order RC low-pass network shown conceptually below:

with the nonlinear capacitor connected from $V_C(t)$ to ground. The input is a sinusoidal voltage source:

$$V_{\text{in}}(t) = V_p \sin(2\pi f t) \tag{5}$$

The output is the capacitor voltage:

$$V_{\text{out}}(t) = V_C(t) \tag{6}$$

For a linear capacitor, the cutoff frequency is:

$$f_c = \frac{1}{2\pi RC} \tag{7}$$

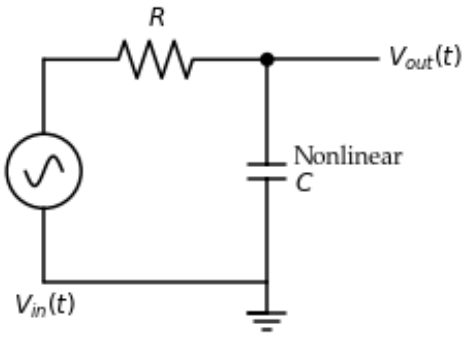

Figure 3: Integrating RC network with a nonlinear capacitor

For the nonlinear capacitor, C varies with instantaneous voltage, so the cutoff frequency is not strictly constant. However, the linearized value using C_0 remains useful as a reference frequency.

4. Why the THD Peak Occurs Near the Transition Band

The nonlinear capacitor modulates circuit current because its incremental capacitance depends on voltage. However, output-voltage distortion is not determined by capacitor nonlinearity alone. It is determined by the interaction between nonlinear current, resistor voltage drop, and the frequency response of the RC network.

The circuit relation is:

$$V_C(t) = V_{\text{in}}(t) - Ri(t) \tag{8}$$

Thus, nonlinear current produces nonlinear voltage error through the resistor.

4.1. Low-Frequency Region: $f \ll f_c$

At low frequency, the capacitor impedance is high and the current is small. The capacitor voltage closely follows the input source:

$$V_C(t) \approx V_{\text{in}}(t) \tag{9}$$

Even though the capacitor experiences a large voltage swing, the current is small. Therefore, the nonlinear voltage error across the resistor is also small:

$$Ri(t) \approx 0 \tag{10}$$

In this quasi-static region, the nonlinear capacitance changes the charge and current required to support the voltage waveform, but it produces little distortion in the measured output voltage.

4.2. Transition Region: $f \approx f_c$

Near the transition band, both conditions occur simultaneously:

- $V_C(t)$ is still large enough to exercise the nonlinear capacitance.
- $i(t)$ is large enough to create a significant voltage drop across R.

This is the region where nonlinear capacitor current is most efficiently converted into output-voltage distortion:

$$V_{\text{error}}(t) = Ri_{\text{nonlinear}}(t) \tag{11}$$

As a result, the output THD tends to peak near the transition band of the network.

4.3. High-Frequency Region: $f \gg f_c$

At high frequency, circuit current may be large, but the capacitor voltage swing is reduced by the low-pass action of the network:

$$|V_C| \ll |V_{\text{in}}| \tag{12}$$

The capacitor is driven over a smaller voltage range, reducing the strength of the capacitance modulation. In addition, harmonic components generated at $2f$, $3f$, and higher frequencies lie deeper in the stopband of the low-pass network. These harmonic voltage components are increasingly shunted by the capacitor and attenuated at the output. Therefore, the output THD can rise near the transition band and then decay at higher frequencies.

5. Correct Nonlinear Capacitor Formulation

A nonlinear capacitor must be modeled through its charge-voltage relation [2], [3]:

$$Q(V) = \int_0^V C_{\text{diff}}(u)\, du \tag{13}$$

and the terminal current must be computed as:

$$i(t) = \frac{dQ(V)}{dt} \tag{14}$$

For the specific case:

$$C_{\text{diff}}(V) = \frac{C_0}{1 + kV^2} \tag{15}$$

the charge relation has a closed-form expression:

$$Q(V) = \frac{C_0}{\sqrt{k}} \tan^{-1}(\sqrt{k}V) \tag{16}$$

This expression is useful because it makes charge conservation explicit. A charge-based simulator should solve the state equation consistently with $Q(V)$, rather than updating voltage from a capacitance value frozen at the beginning of a finite time step.

6. Incorrect Instantaneous $C(V)$ Update

The continuous-time identity

$$i(t) = C_{\text{diff}}(V)\frac{dV}{dt} \tag{17}$$

is not by itself wrong when $C_{\text{diff}}(V) = dQ/dV$. The modeling trap appears when a transient solver or behavioral model updates voltage using a locally frozen capacitance. For a fixed-step update, this produces a discrete equation:

$$V_n = V_{n-1} + \frac{\Delta t}{C_{\text{diff}}(V_{n-1})} i_n \tag{18}$$

This update is not equivalent to the charge relation:

$$Q(V_n) - Q(V_{n-1}) = \int_{t_{n-1}}^{t_n} i(t)\, dt \tag{19}$$

The error arises because the capacitance is evaluated at the old voltage and treated as constant during the time step, even though the voltage changes during that same step. This numerical method injects or removes charge incorrectly and can produce step-size-dependent harmonic content. The magnitude depends on the solver, time step, waveform, and model parameters; it must be established by convergence testing rather than assumed.

7. Simulation Example

The following controlled example compares two capacitor models in the same RC network:

1. **Charge-conserving model:** capacitor defined by $Q(V)$.
2. **Naive instantaneous model:** capacitor updated from locally frozen $C_{\text{diff}}(V)$.

Nominal parameters: $R = 1\,\text{k}\Omega$, $C_0 = 1\,\mu\text{F}$ ($f_c = 159.2\,\text{Hz}$), $V_p = 5\,\text{V}$, $k = 0.5\,\text{V}^{-2}$, $n = 2$. The THD is computed at the output voltage $V_C(t)$ for harmonics up to the fifth order:

$$\text{THD}_5 = \frac{\sqrt{|V_2|^2 + |V_3|^2 + |V_4|^2 + |V_5|^2}}{|V_1|} \tag{20}$$

where V_1 is the fundamental output-voltage component and V_2 through V_5 are harmonic components. A reproducible nonlinear THD sweep should specify settling cycles before FFT analysis, the number of analyzed cycles, sampling interval, FFT window or coherent-sampling method, harmonic extraction method, and a convergence check versus decreasing time step.

8. Simulation Results

The charge-conserving model produces a physically plausible THD curve. The simulated THD rises toward the RC transition region and then falls at higher frequency as the capacitor voltage swing and harmonic output components are attenuated. The naive fixed-step $C(V)$ update tracks the same broad trend, but its result remains step-size dependent and should not be interpreted as a physical dielectric prediction without convergence.

A diagnostic is to repeat the sweep with progressively smaller time steps. Physical distortion should converge, while numerical distortion caused by charge error will change significantly.

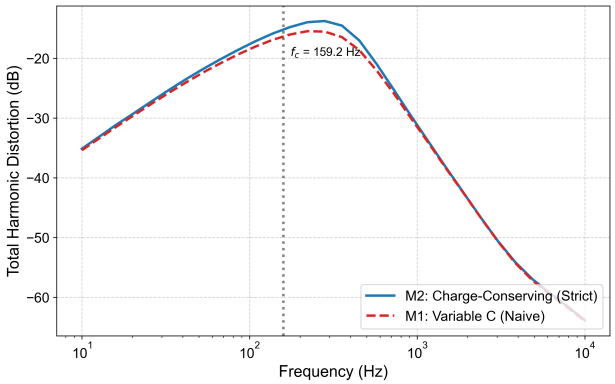

Figure 4: THD vs. Frequency. Comparison between the charge-conserving Q(V) and naive C(V) models.

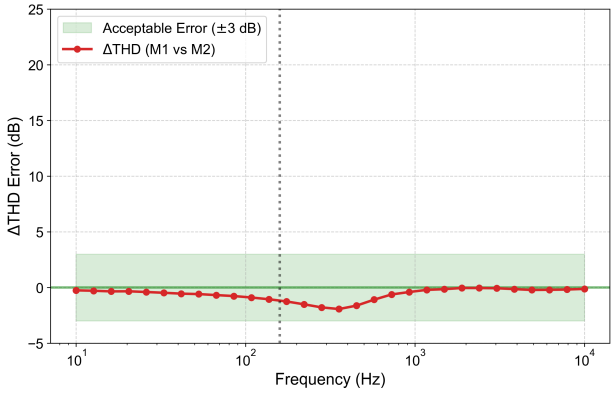

Figure 5: Simulation difference ΔTHD for the deliberately coarse naive update. The illustrated ±3 dB band is a visual reference, not an acceptance criterion. The result is a numerical-model diagnostic rather than a dielectric property.

9. Design Implications

- **Do Not Assume Worst-Case THD Occurs at Maximum Frequency:** For a nonlinear capacitor in an RC low-pass network, the worst output-voltage distortion may occur near the transition band.
- **Voltage Swing Matters:** The distortion is strongly amplitude-dependent.
- **Use Class I Dielectrics Where Linearity Matters:** When distortion performance is critical, Class I dielectrics such as C0G/NP0 are preferred.
- **Verify Nonlinear Capacitor Models:** Confirm that the behavioral capacitor model is charge-based.
- **Validate with Time-Step Convergence:** If simulated THD changes significantly when the maximum time step is reduced, the result should be treated as suspect.

10. Limitations

This note uses a simplified voltage-dependent capacitance model. Real Class II MLCCs exhibit additional effects not captured here, including temperature dependence, DC-bias history, aging, dielectric relaxation, frequency dispersion, dielectric absorption, package-dependent electromechanical behavior, and manufacturing variation.

The numerical values in this note should therefore be treated as a controlled example, not as a universal prediction for all X7R or X5R capacitors. Final capacitor selection should be validated with vendor data and, where distortion is critical, bench measurement under the actual signal amplitude, bias, frequency range, and PCB conditions.

11. Practical Checklist

Before approving a Class II ceramic capacitor in a precision analog signal path, verify the following:

- Is the capacitor exposed to large AC voltage swing?
- Is the signal frequency near an RC transition band?
- Is THD, SFDR, or low-level linearity important in this node?
- Would a C0G/NP0, film, or larger derated capacitor be more appropriate?
- Does the simulation model conserve charge?
- Has the THD result been checked against time-step convergence?
- Is the result supported by vendor data or bench measurement?

12. Conclusion

Voltage-dependent capacitance in Class II ceramic capacitors can produce harmonic distortion in analog signal paths. In a first-order RC low-pass network, the maximum output-voltage THD is often found near the transition band. Updating a voltage-dependent capacitor from a locally frozen $C(V)$ value can violate charge conservation and generate non-physical harmonics. For precision analog design, Class II ceramic capacitors should be used with caution in large-signal or distortion-sensitive nodes.

Open resources and engineering review

The public release package includes this note, the source code, the controlled simulation inputs, and reproduction instructions:

- Application-note page: highsnr.org/application-notes/an-001
- Source code: github.com/DrBorisKuznetsov/cvfreq-distortion-study
- Related research preprint: doi.org/10.31224/7436

HighSNR Lab performs independent nonlinear-model validation and distortion-oriented design review for precision analog signal paths. To discuss a component model, circuit, or measurement study, contact info@highsnr.org.

References

[1] J. Caldwell, "Signal distortion from high-K ceramic capacitors," *EDN*, vol. 58, no. 12, pp. 22–27, 2013.

[2] D. E. Ward and R. W. Dutton, "A charge-oriented model for MOS transistor capacitances," *IEEE Journal of Solid-State Circuits*, vol. 13, no. 5, pp. 703–708, Oct. 1978.

[3] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*. Boston, MA: Kluwer Academic Publishers, 1998.

[4] Murata Manufacturing Co., Ltd., "Voltage Characteristics of Capacitors," Application Note.

[5] Murata Manufacturing Co., Ltd., "GRM155R60J105KE19 Product Data," https://www.murata.com/en-us/products/productdetail?partno=GRM155R60J105KE19%23.

[6] Murata Manufacturing Co., Ltd., "SimSurfing: Simulation Data for Electronic Components," https://www.murata.com/en-us/tool/simsurfing, accessed July 27, 2026.

[7] B. Kuznetsov, "Frequency-Dependent Distortion in Class II Ceramic Capacitors: Physics and Simulation Traps," engrXiv, 2026, doi: 10.31224/7436.

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