



Third Harmonic Distortion in a 10 μ F X7R RC Filter at Zero Applied DC Bias

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Key Results

A 10 μ F X7R capacitor can introduce substantial distortion in a signal path even when no DC bias is applied. We measured ten Fenghua 1206B106K100NT capacitors from one tape at 19.8 Hz. The measured third harmonic of current averaged **-49.8 dBc**. A circuit calculation gives **-44.6 dBc, or 0.59%, across the capacitor** at approximately 0.43 V RMS.

The individual capacitor means ranged from -50.1 to -49.3 dBc; the 29 complete measurement runs ranged from -50.5 to -49.0 dBc. Third-harmonic distortion was about 3 dB higher in the first analysis window than in the interval from 35 to 51 s. The short-circuit control had an absolute third-harmonic level approximately 65 dB below the capacitor measurements.

These results support a practical design check: calculate the AC voltage across the capacitor, estimate how its nonlinear current couples into the output, and compare that contribution with the distortion budget. The measurements cover one operating point. The circuit examples in this note are model-based estimates; transfer to another circuit was not experimentally validated.

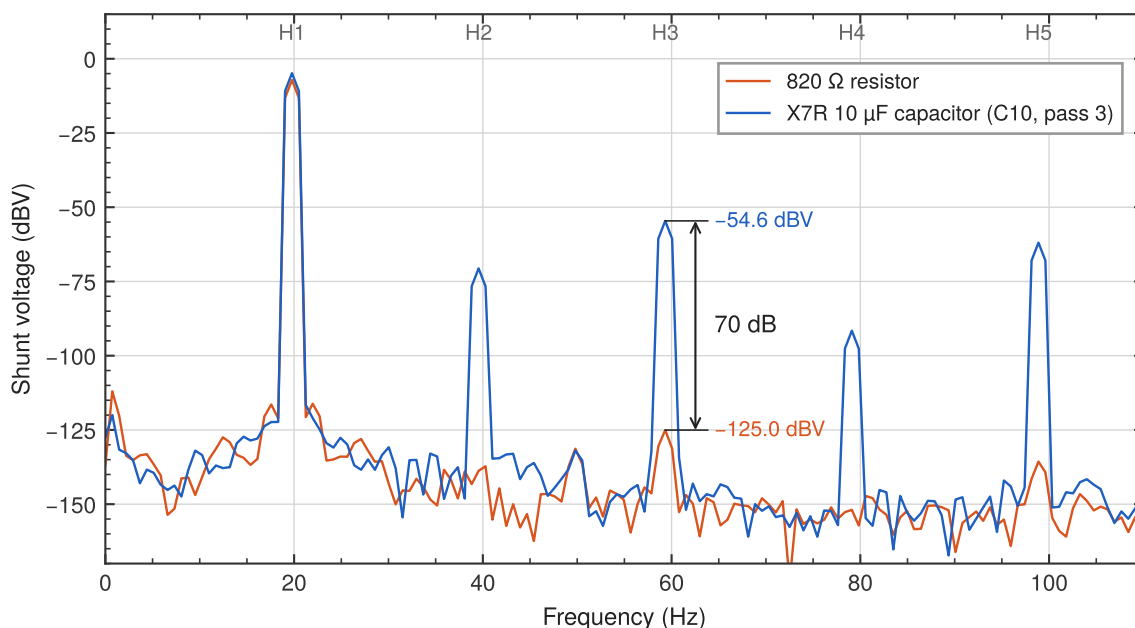


Figure 1. Shunt-voltage spectra with an 820 Ω resistor and a 10 μ F X7R capacitor in the same fixture. The capacitor raises the absolute third-harmonic level by approximately 70 dB relative to this resistor trace. Capacitor: C10, pass 3, window 30. Resistor: window 8 of the final control pair.

1 Why Zero DC Bias Does Not Ensure Low Distortion

Class II ceramic capacitors offer high capacitance in a small package, but their electrical response depends on the applied voltage. Checking capacitance loss under DC bias does not establish linearity under an AC signal. A sinusoidal voltage can produce harmonic current even when its mean is zero.

For a designer using an X7R capacitor in an RC filter or an AC-coupling network, the relevant quantity is the distortion at the signal output. That quantity depends on both the capacitor and the surrounding impedances. This note reports a measured example, develops a first-order circuit model for interpreting it, and provides a procedure for testing another component.

Throughout this note, **zero applied DC bias** means that no intentional DC voltage was applied. A preliminary DC measurement found no stable millivolt-scale offset in the configuration tested. Absolute DC voltage was not independently verified after the acquisition system changed to direct USB streaming; Section 8.6 describes that limitation.

2 Test Circuit and Operating Point

The QA403 generator drives the capacitor and a current-sense resistor in series. The analyzer measures the differential voltage across the sense resistor. This voltage is proportional to the series current. The low-pass response of interest is the voltage across the capacitor, regardless of where that capacitor is drawn in the series loop.

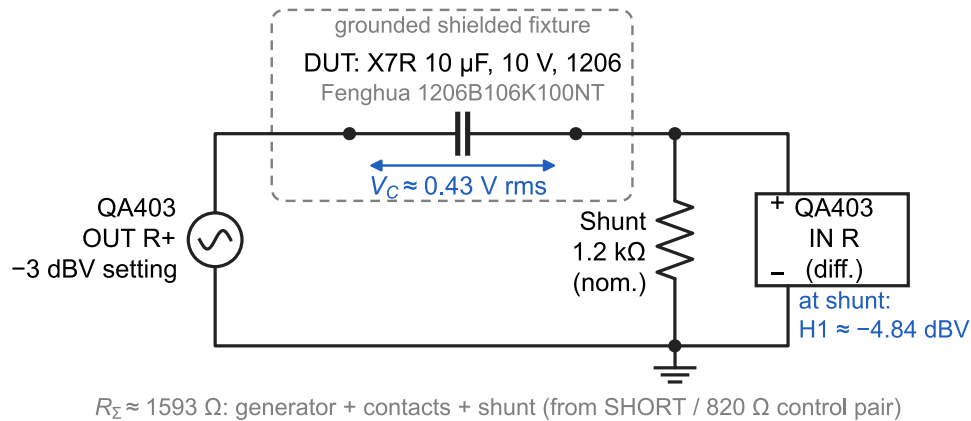


Figure 2. Test circuit using the QA403 right-channel output and differential right-channel input. The 1.2 k Ω sense resistance is nominal. The fundamental voltage marked at the sense resistor is the mean of 29 complete runs; the capacitor voltage is calculated.

Parameter	Value
Capacitor	Fenghua 1206B106K100NT, X7R, 10 μ F, 10 V, 1206
Total series resistance, R_{Σ}	Approximately 1593 Ω , inferred from short-circuit and resistor controls
Excitation frequency	19.775390625 Hz
Calculated low-pass corner	Approximately 11 Hz
Calculated R_{Σ}/X_C	Mean 1.80; range 1.76 to 1.85
Calculated capacitor voltage, V_C	Approximately 0.43 V RMS
Calculated effective capacitance, C_{eff}	Mean 9.13 μ F; range 8.91 to 9.43 μ F

The calculated quantities use 26 runs with a usable phase reference. The voltage estimate also uses the nominal 1.2 k Ω sense resistor in parallel with the analyzer's assumed 100 k Ω input resistance. The sense resistor was not independently calibrated. Section 8.4 gives the extraction method and assumptions.

The operating frequency is about 1.8 times the calculated corner frequency. In this region, a substantial AC voltage remains across the capacitor. Its nonlinear response therefore matters even though the network attenuates the fundamental.

From Measured Current to Capacitor Voltage

Let I_1 and I_3 denote the fundamental and third-harmonic current phasors. With source harmonic E_3 and total external series impedance Z_Σ , Kirchhoff's voltage law gives

$$V_{C3} = E_3 - Z_\Sigma(3\omega)I_3.$$

For negligible E_3 and a resistive series impedance, $V_{C3} \approx -R_\Sigma I_3$. At the fundamental, $V_{C1} = Z_C(\omega)I_1$. Consequently,

$$\frac{|V_{C3}|}{|V_{C1}|} \approx \frac{|I_3|}{|I_1|} \frac{R_\Sigma}{|Z_C(\omega)|} \approx \frac{|I_3|}{|I_1|} \frac{R_\Sigma}{X_C}.$$

The last approximation treats the capacitor impedance as predominantly reactive. With $R_\Sigma/X_C \approx 1.80$, the voltage harmonic ratio is about 5.1 dB higher than the current harmonic ratio. The calculation across the 26 usable runs gives a mean of **-44.6 dBc** at the capacitor, with a range of **-45.3 to -43.8 dBc**.

The controls establish a large measurement margin: the absolute H3 level with a short is about 65 dB below that with a capacitor. Under the assumption that this residual contributes unchanged and coherently, its worst-case effect is about 0.005 dB. This comparison does not independently bound every load-dependent or contact-related error.

3 Measured Results

Ten capacitors from one tape were measured in three passes. Each part was removed and reinstalled between passes; the order within each pass was randomized in advance. Four short-circuit/resistor control pairs bracketed the passes. The series comprised 30 capacitor mountings and eight control mountings over approximately 3.8 hours.

The archived ADC file for C04 in pass 3 is incomplete. That run is excluded from the primary statistics, leaving 29 complete capacitor runs. C04 therefore has two accepted runs in Table 1; the other parts have three.

Table 1. Harmonic ratios by capacitor, referenced to the fundamental current.

Part	H3/H1 (dBc)	H2/H1 (dBc)	First-window H3/H1 (dBc)
C01	-50.1	-64.6	-46.8
C02	-49.9	-62.4	-46.7
C03	-49.3	-64.7	-46.3
C04	-49.8	-64.0	-46.8
C05	-49.8	-64.3	-46.7
C06	-49.5	-64.3	-46.5
C07	-49.5	-65.4	-46.3
C08	-49.5	-67.0	-46.5
C09	-50.0	-65.5	-46.9
C10	-50.1	-64.8	-46.8

H3 and H2 are averages in decibels over windows 21 through 30, followed by an average across the accepted runs for each part. The windows cover approximately 35 to 51 s after excitation begins. The last column is the median of the valid first-window results for each part; that window spans 0.34 to 1.71 s.

The first windows of C01 and C10 in pass 1 and C08 in pass 2 are excluded from the last column. They exhibit acquisition anomalies: the fundamental is 1.3 to 4.5 dB lower and its phase differs from later windows. Their later-window harmonic ratios remain in the primary statistics. Those three runs are also excluded from calculations that require an absolute phase comparison with a separate short-circuit run.

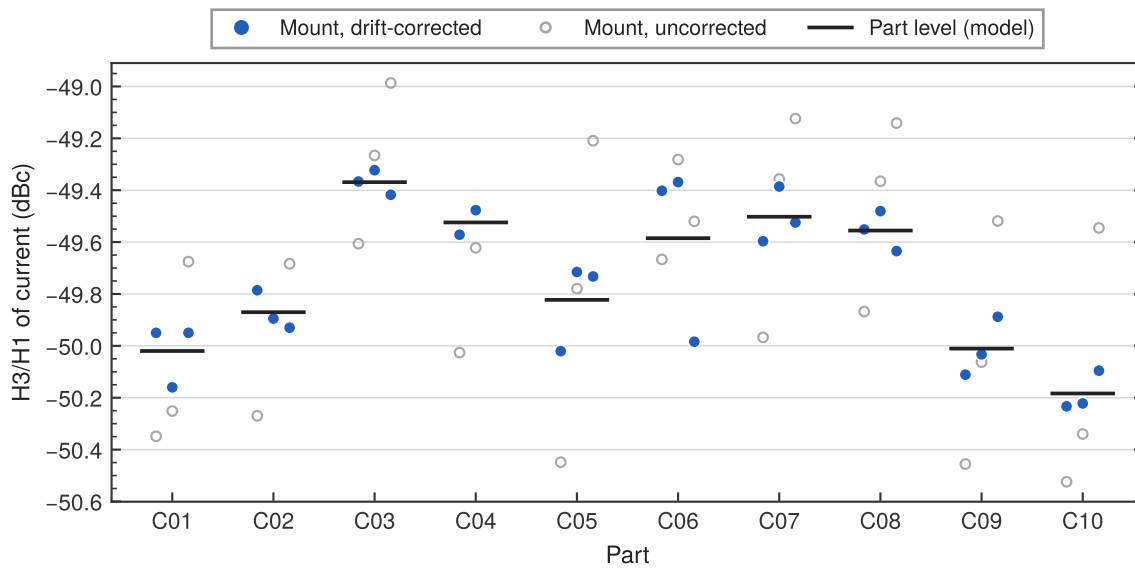


Figure 3. Third-harmonic current ratios by part. Filled circles are individual runs corrected to the mean measurement time using the fitted common slope of +0.27 dB/h. Open circles show the uncorrected measurements. Horizontal bars are fitted part levels. C04 has two complete runs.

The mean across 29 complete runs is -49.75 dBc. The individual part means span 0.85 dB, and each of the ten observed means lies within 0.5 dB of their average. The effect is therefore large enough that any of these ten parts would reveal the same basic design issue at this operating point. This does not establish a sampling rule for the rest of the tape or for production acceptance.

A separate measurement on October 14, 2026, using a part from the same tape, reported -49.47 ± 0.10 dBc. Its acquisition method and record duration differed. It provides agreement in observed magnitude, rather than an identical-protocol replication.

For perspective, the TI ADS127L11 data sheet lists a typical THD of -120 dB at a 1 kHz input near full scale [4]. That specification includes nine harmonics and uses different signal conditions. It illustrates the distortion scale available from a precision ADC; it is not a direct comparison with this 19.8 Hz capacitor measurement.

4 Estimating Distortion in Another Circuit

The measured current ratio is specific to the test network. A useful first-order model separates the capacitor's nonlinear excitation from the linear response of the surrounding circuit.

Equivalent Harmonic Source

For weak distortion, represent the capacitor at the third harmonic by a linear capacitance C_0 in parallel with a harmonic current source. Define the nonnegative coefficient k_3 as

$$k_3 = \frac{|Q_{nl,3}|}{C_0 |V_{C1}|}, \quad |I_{s3}| = 3\omega C_0 |V_{C1}| k_3.$$

Here $Q_{nl,3}$ is the nonlinear third-harmonic charge generated under a purely sinusoidal capacitor voltage at the specified amplitude, frequency, DC bias, temperature, and elapsed excitation time. The expression specifies the source magnitude. Its phase must also be retained when combining it with other harmonic sources.

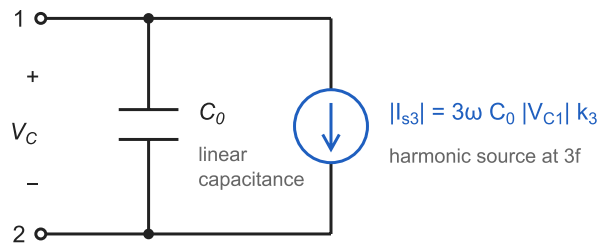


Figure 4. A linear capacitance in parallel with an equivalent third-harmonic current source. The source represents the nonlinear response at the specified operating point.

This definition differs from the total charge harmonic ratio in a loaded circuit. For total charge, $I = dQ/dt$ gives $|Q_3/Q_1| = |I_3/I_1|/3$. The linear capacitance also carries harmonic current when the circuit develops a third-harmonic voltage.

For a predominantly capacitive DUT and resistive external impedance, write $x = \omega C_0 R_\Sigma$. The measured current ratio then gives

$$k_3 \approx \frac{|I_3|}{|I_1|} \frac{\sqrt{1 + 9x^2}}{3}.$$

The data yield a mean $20 \log_{10}(k_3)$ of **-44.4 dB**, with a range of -45.1 to -43.6 dB across the 26 runs used for the circuit calculation. This estimate applies near 0.43 V RMS and 19.8 Hz. The experiment did not measure the dependence of k_3 on amplitude or frequency.

Low-Pass RC Filter

For a series resistance R feeding a shunt capacitor, with the output taken across that capacitor and no additional output load,

$$\frac{|V_{\text{out},3}|}{|V_{\text{out},1}|} \approx k_3 \frac{3x}{\sqrt{1+9x^2}}, \quad x = \omega C_0 R.$$

Above the corner frequency, the voltage harmonic ratio approaches k_3 . Well below the corner, where $3x \ll 1$, the ratio approaches $3xk_3$. Both statements assume that k_3 has been evaluated at the actual capacitor voltage.

Example A. Consider a 1 k Ω low-pass filter using this capacitor at 19.8 Hz, driven by 0.64 V RMS. With $C_0 = 9.13 \mu\text{F}$, $x \approx 1.13$ and $V_C \approx 0.42$ V RMS, close to the measured operating point. Applying the extracted coefficient gives an output H3 ratio of approximately **-44.8 dBc**. A design requiring a capacitor contribution below -100 dBc would have ample reason to reject this component for that operating point. The numerical estimate remains conditional on the model and the small change in capacitor voltage.

AC-Coupling Capacitor

For a series coupling capacitor feeding a resistive load R , with negligible source resistance and $X_C \ll R$, the output is taken across the load. In that limit,

$$\frac{|V_{\text{out},3}|}{|V_{\text{out},1}|} \approx k_3 \frac{|V_{C1}|}{|V_{\text{in},1}|}.$$

Only a fraction of the input voltage appears across the capacitor. This reduces the coupling of its harmonic source into the output. The nonlinear source itself may also decrease with capacitor voltage, but that dependence requires measurement or a validated material model.

Example B. A 10 μF coupling capacitor feeding 10 k Ω from a 1 V RMS source at 19.8 Hz has approximately 0.088 V RMS across it when $C_0 = 9.13 \mu\text{F}$. The circuit factor alone provides about 21 dB of attenuation. If k_3 scales as V_C^2 , extrapolation from the measured point gives approximately **-93 dBc** at the output. If it scales as V_C , the estimate is approximately **-79 dBc**. These are two assumed laws, not measured predictions or bounds. Their 14 dB difference shows why a measured amplitude dependence is needed before accepting the part for this application.

Conditions for Applying the Model

Use the extracted k_3 only for comparable capacitor voltage, frequency, bias, temperature, and excitation history. The surrounding network must be linear, its impedances at f and $3f$ must be known, and harmonic feedback must be small enough for the first-order approximation to hold. For another topology, solve the linear network at $3f$ with the equivalent current source inserted at the capacitor terminals. A scalar magnitude is sufficient only when phase-dependent addition with other distortion sources is negligible.

5 Variation Between Parts and Repeated Mountings

The raw results contain both differences between parts and a common change over the measurement session. An ordinary least-squares fit with one level per part and a linear time term gives a slope of **+0.27 dB/h**. After that correction, the standard deviation of the fitted part levels is **0.27 dB**, and the residual standard deviation is **0.15 dB**. A fit using part and pass instead of part and time gives a residual standard deviation of **0.19 dB**.

The conditional F-test for part differences after accounting for linear time gives $p \approx 4 \times 10^{-5}$. These estimates depend on the additive model and its error assumptions. The residual includes remounting, contacts, and any departure from the assumed drift. It does not isolate fixture repeatability.

For an initial assessment of distortion magnitude at this operating point, the observed variation is small compared with the separation between the DUT and the controls. Qualification of another tape, lot, or

manufacturer requires its own measurements. Neither the observed 0.85 dB span nor the fitted standard deviation is a guaranteed production limit.

The common increase during the session may reflect changing environmental conditions. Temperature was not logged, and elapsed time was not separated from excitation history. A temperature explanation therefore remains a hypothesis.

6 Distortion Changes After Excitation Begins

The first valid analysis windows give a median H3/H1 current ratio of approximately -46.6 dBc. The late-record metric is approximately -49.8 dBc. From the first to the last window, valid records decrease by roughly 3.0 to 3.5 dB. Near the end of the recording, H3/H1 is still decreasing at approximately 0.025 to 0.030 dB/s.

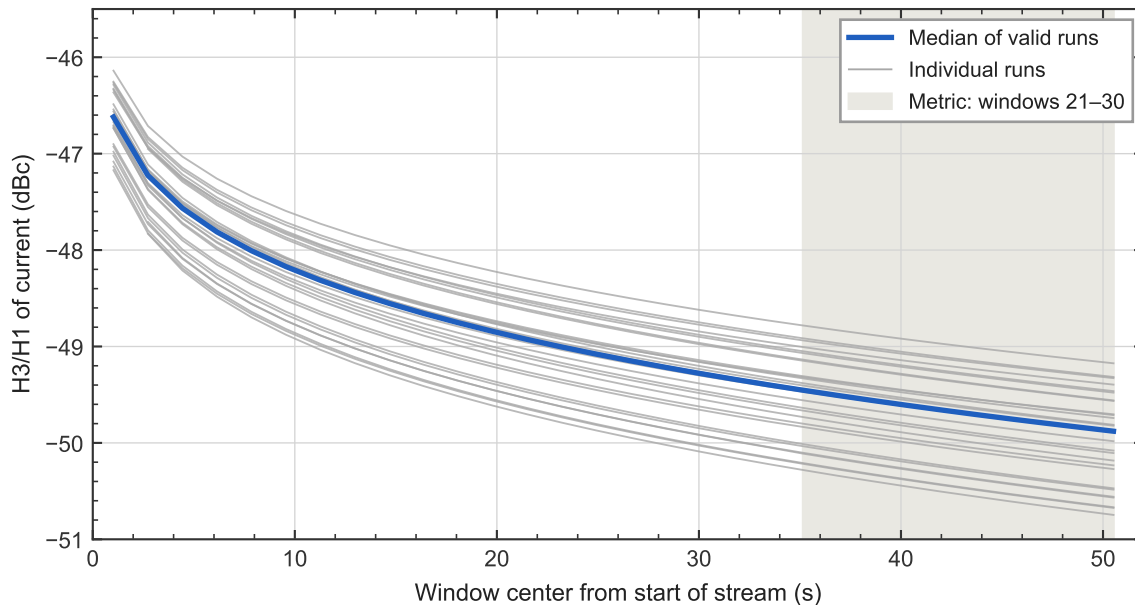


Figure 5. Third-harmonic current ratio versus time for the 29 complete capacitor runs. Each run followed a 180 s interval with excitation off. The shaded region identifies windows 21 through 30. The median at the first window uses 26 valid values because three anomalous first windows are omitted. Time is measured from the start of the digital stream; the first window spans 0.34 to 1.71 s.

The decay recurs across the measured parts and after repeated off intervals. Its physical mechanism was not established. The reported late-record metric is a defined observation interval, not a demonstrated steady-state value.

Specify both the off interval and the measurement time when comparing parts or reproducing these results. A measurement made a few seconds after turn-on will not be directly comparable with one made near the end of a 50 s record. The first-window result averages 1.37 s of a sinusoidal test; it does not establish instantaneous distortion or a bound for pulses and short bursts.

7 Second Harmonic Observations

An ideal charge-voltage characteristic with odd symmetry produces only odd harmonics under symmetric excitation. The measured parts also produced H2, with mean current ratios from approximately -62 to -67 dBc. H2 was 12 to 18 dB below H3 and varied between parts.

The short-circuit and resistor controls did not show a comparable H2 component. That observation is con-

sistent with a contribution associated with the installed DUT, but it does not identify the mechanism. The preliminary DC check covered only one part and preceded the change in acquisition method. Residual DC bias and load-dependent measurement effects are therefore not fully excluded. Intrinsic asymmetry of individual capacitors is one possible explanation.

For design purposes, absence of intentional DC bias is not sufficient grounds for omitting H2 from the distortion budget. Its origin and bias dependence require separate characterization.

8 Measurement Method

8.1 Hardware and Connections

Measurements were made on October 20, 2026, using a QuantAsylum QA403. The R+ generator output drove the test loop, and the differential R input sensed the voltage directly across the current-sense resistor through a twisted pair. The output range was -2 dBV, the input range was 0 dBV, and the generator setting was -3 dBV.

A Python program used WinUSB/libusb1 for continuous ADC and DAC streaming. It applied the analyzer's factory EEPROM calibration; firmware and EEPROM contents were not modified. QA40x version 1.223 was used for preliminary checks and the DC measurement, rather than for the main acquisition. Analysis used Python 3.13, NumPy, and Matplotlib.

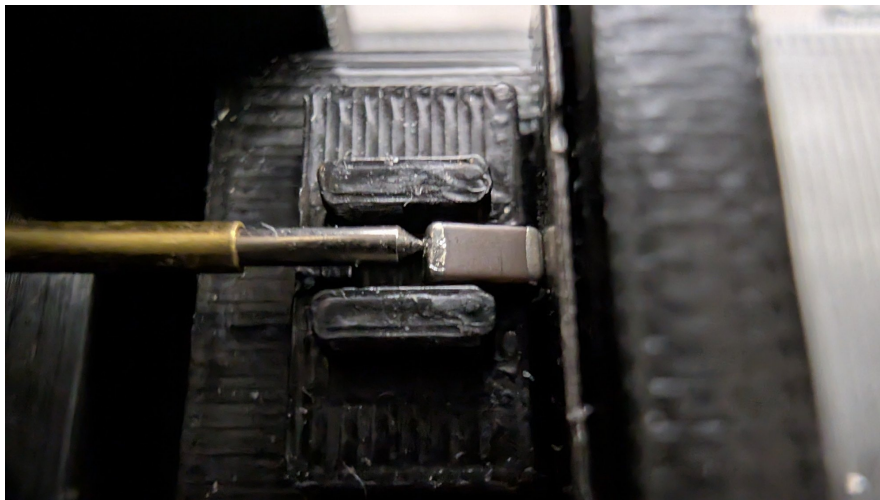


Figure 6. A 1206 capacitor held by a spring-loaded contact in the test fixture. The photograph shows the mechanical contact arrangement.

The fixture uses spring-loaded needle contacts in a 3D-printed housing with three BNC connections. Its shield is connected to the measurement ground. Spring loading helps maintain contact force, but contact-force variation was not separately measured. The sense resistor is a general-purpose through-hole resistor with a nominal value of 1.2 k Ω .

The control loads were a short and an 820 Ω resistor in parallel with 10 M Ω . The parallel combination measured 820.04 Ω with the multimeter. The second resistor provides the thickness needed by the fixture; the assembly is referred to as 820 Ω in this note.

For the preliminary DC check, a UNI-T UT61E in DC mV mode was connected across the DUT through a 1 M Ω / 2.2 μ F low-pass filter using a CBB22 film capacitor. The meter resolution was 10 μ V. Its leads were disconnected during the main series; the filter remained on the board. Ambient temperature was neither controlled nor logged.

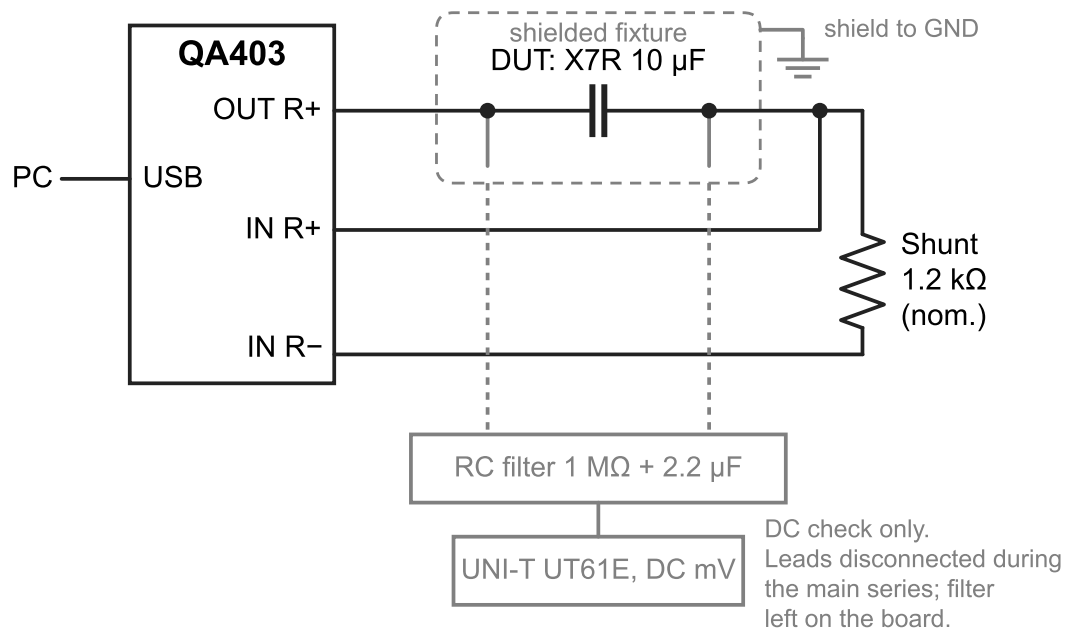


Figure 7. Analyzer, fixture, current-sense resistor, and preliminary DC measurement connections. The gray circuit was used only for the DC check. Multimeter leads were disconnected during the main series.

8.2 Excitation and Acquisition

Parameter	Setting
Sample rate	48,000 samples/s
Excitation frequency	$27 \times 48,000 / 65,536 = 19.775390625$ Hz
H2 and H3 frequencies	39.551 Hz and 59.326 Hz
DUT record	Approximately 52 s of continuous ADC and DAC data
Analysis window	65,536 samples, 1.365 s, periodic Hann window
DUT analysis	30 windows, spaced 81,920 samples or 1.707 s apart
DUT window centers	1.02 to 50.52 s
Control analysis	Eight windows, with centers from 1.02 to 12.97 s

The fundamental and its harmonics fall on integer FFT bins. Analysis windows do not overlap. The saved stream includes the samples between windows.

For each run, the operator installed the load and confirmed readiness. The generator remained off for 180 s, then excitation and continuous acquisition began. After the record, the program sent zeros to the DAC and issued an output-off command. A subsequent capture checked for residual excitation at the sense resistor. Instrument control, acquisition, and calculation were automated; the operator changed the physical configuration.

8.3 Controls and Repeated Runs

A short-circuit/resistor pair was measured before the first pass, between passes, and after the final pass. The accepted control rule required H3 to remain no more than 1 dB above its historical reference and a margin of at least 40 dB against the calculated leakage of 48 to 52 Hz interference into the H3 bin.

This rule was adopted after the first controls had been inspected and before capacitor measurements began. The original target was a ± 1 dB band around historical control values and a 48 to 52 Hz line below -135 dBV. The change is relevant when interpreting the controls as part of the experimental protocol.

C02 and C04 were remeasured in pass 3 after changes in H1 were observed. No numerical H1 threshold had been specified in advance. Decisions were made during the experiment, and the earlier attempts remain in the archive. The cause of the H1 changes was not established.

8.4 Signal Processing and Circuit Extraction

Each window is mean-subtracted and multiplied by a periodic Hann window. Complex H1 through H5 are computed at the exact harmonic frequencies. Normalization by $\sqrt{2}/\sum w$ gives RMS amplitude. The reported ratio for harmonic n is

$$D_n = 20 \log_{10} \left(\frac{|H_n|}{|H_1|} \right) \quad \text{dBc.}$$

The primary run metric is the mean of D_3 over windows 21 through 30, whose centers span 35.2 to 50.5 s. This interval was specified before measurement. Part means are averages of the accepted run metrics. The first-window metric uses the window from 0.34 to 1.71 s, centered at 1.02 s.

Let V_{SHORT} and V_R be the complex fundamental voltages measured across the sense resistor with the short and the $820.04 \, \Omega$ control load. The inferred source-plus-sense impedance is

$$Z_{\Sigma} = R_{\text{ctrl}} \frac{V_R}{V_{\text{SHORT}} - V_R}, \quad R_{\text{ctrl}} = 820.04 \, \Omega.$$

For a DUT run with fundamental sense voltage V , the extracted impedance is

$$Z_C = Z_{\Sigma} \left(\frac{V_{\text{SHORT}}}{V} - 1 \right), \quad C_{\text{eff}} = \frac{1}{\omega |\text{Im } Z_C|}.$$

The calculation uses the bracketing controls and assumes a stable linear source, a common ADC scale, and a reproducible phase reference. The three phase-anomalous runs identified in Section 3 are excluded, leaving 26 runs. The extracted ratios do not require the sense-resistor value; the capacitor voltage does. For that voltage calculation, the nominal $1.2 \, \text{k}\Omega$ resistor is placed in parallel with $100 \, \text{k}\Omega$.

The capacitor-side harmonic calculation assumes that Z_{Σ} is resistive and unchanged between f and $3f$, neglects source H3, and uses C_{eff} as C_0 . The simplified formulas in Sections 2 and 4 show the predominantly reactive limit. Choosing the control pair before or after a pass changes the calculated harmonic ratios by at most 0.002 dB and C_{eff} by at most $0.13 \, \mu\text{F}$. Those sensitivity checks do not include uncertainty in nominal sense resistance or model assumptions.

Part differences and drift are evaluated with ordinary least squares using run completion time. The published code includes the part-plus-time and part-plus-pass fits and the conditional F-test.

8.5 Residual Harmonics and Headroom

Table 2. Final control pair and representative DUT levels at the analyzer input.

Load	H3/H1 (dBc)	Absolute H3 (dBV)
Short circuit	-115.6	-119.1
$820 \, \Omega$ resistor	-117.2	-124.4
$10 \, \mu\text{F}$ X7R capacitor	Approximately -50	Approximately -55 to -54

The maximum recorded ADC peak was 0.63 of full scale. No overload was observed. The control results support detection of the DUT-associated H3 with a large margin; they do not constitute a complete uncertainty budget for its attribution to a particular physical mechanism.

8.6 Preliminary DC Check

C01 was measured for 30 s with excitation off, 30 s on, and another 30 s off. The mean readings over the last 10 s of each interval were **-19.5, -50.5, and -40.0 μV** , respectively. The on-minus-initial-off change was approximately $-31 \mu\text{V}$, comparable in scale with the $-20.5 \mu\text{V}$ change between the two off intervals.

This check used the stock QA40x application before acquisition changed to direct USB streaming. The filter's DC transfer and drift were not calibrated. These readings describe the preliminary measurement path; they do not establish the absolute DC voltage across the DUT throughout the main series.

8.7 Data Integrity and Scope

The archive contains ADC and DAC streams, per-window complex H1 through H5, calibration data, command logs, acquisition settings, source-code snapshots, and file hashes. The incomplete C04 pass 3 ADC file is preserved as received and is identified in the integrity amendment. Its stored full-run result is excluded from the primary statistics; 29 capacitor runs and all eight controls are fully supported by the retained raw data.

The main series covered one frequency and one excitation setting. The planned amplitude and frequency sweeps were not performed. Their absence limits the extrapolations in Section 4 and does not affect the observation of substantial H3 at the measured operating point.

9 Applying the Method to Your Component

Calculate the capacitor voltage in the intended circuit before setting up the test. Use the expected capacitance under the actual bias and signal conditions. A generator setting alone does not specify the voltage across a capacitor in a loaded network.

1. Choose an excitation frequency on an integer FFT bin and verify the actual input channel with a known signal.
2. Measure a short and a linear resistor of order X_C in the same fixture. Compare absolute harmonic levels at the analyzer input, not only dBc ratios with different fundamentals.
3. Ground the fixture shield and record the line-frequency interference. Evaluate its leakage into the harmonic bins for the chosen window and record length.
4. Verify that the generator is physically off during the rest interval. In our preliminary QA40x 1.223 REST tests, `Gen1/Off` did not remove the output; `OutputSource/Off` did. Check the residual tone directly for the control method being used.
5. Specify the rest interval and analysis interval before collecting comparative data. This experiment used 180 s off and approximately 52 s of recording.
6. Make at least three independent mountings and randomize the order when comparing several parts. Log temperature near the fixture.
7. Report the first valid window separately from the predefined late-record metric. Retain raw streams, settings, calibration, and reasons for any exclusions.

As a practical target, keep the control H3 at least 40 dB below DUT H3 in absolute amplitude. If that residual transfers unchanged into the DUT measurement, worst-case coherent addition changes the result by less than 0.1 dB. This is a recommended measurement margin, distinct from the leakage criterion used to accept this experiment's controls.

For the tested part at approximately 0.43 V RMS and 19.8 Hz, the calculated output H3 of a comparable low-pass filter is far above a -100 dBc design target. For a coupling capacitor operating at much lower voltage, measure the amplitude dependence before deciding whether the part meets the budget. The model

provides a way to use those measurements without treating a single test-network current ratio as a universal component specification.

10 Data and References

[1] Experimental data and reproducibility package. Boris Kuznetsov, HighSNR Lab, version 1.0.1, 2026. doi:10.5281/zenodo.23528005. The core archive contains processed data, analysis code, figures, integrity records, and the full measurement report in Russian. The selected-raw archive contains 43 directories: 38 accepted mountings, three documented attempts, and two DC checks. Data are licensed under CC BY 4.0; code is licensed under MIT. Reproduction instructions and verification scripts are included in the archives.

[2] Related application note. *Frequency-Dependent Distortion in Class II Ceramic Capacitors*, HighSNR Lab, AN-001. highsnr.org/application-notes/an-001.

[3] Related preprint. *Frequency-Dependent Distortion in Class II Ceramic Capacitors: Physics and Simulation Traps*. engrXiv. doi:10.31224/7436.

[4] ADC comparison. Texas Instruments, *ADS127L11 400-kSPS, Wide-Bandwidth, 24-Bit, Delta-Sigma ADC*, data sheet. The cited typical THD is -120 dB with a 1 kHz input at -0.2 dBFS, OSR 64, 200 kSPS, and nine harmonics. ti.com/lit/ds/symlink/ads127l11.pdf.

Acknowledgment

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