# Design Review Report

8-Channel Precision Battery Cell Voltage Acquisition Front-End

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|---|---|---|---|
| Report ID | SNR-R-2607, Rev. 2 | Reviewed by | B. Kuznetsov, HighSNR Lab |
| Date | 2026-07-24 | Engagement | Expert Audit, SOW SNR-Q-2607 |
| Object | `battery_tester_rev_d.kicad_sch`, rev. D of 2026-07-23 | Client brief | Symptoms S1–S7, questions Q1–Q5 |
| File MD5 | `369076eafce2a899c5193ae73f1f1691` | Status | **Corrected demonstration report** |

This is a public demonstration of the HighSNR Lab review format. The design, the client persona, and the "measured" symptoms form a constructed teaching case built on a HighSNR reference design; no client materials were used. Rev. 2 corrects the component data, distinguishes demonstrated mechanisms from unverified hypotheses, and separates conservative limits from statistical performance estimates.

## 1 Executive Summary

The architecture is viable for precision dc logging, but the submitted signal chain does not support the stated accuracy across temperature and sample rate. Two defects require a schematic change, and three additional mechanisms require bench validation before they can be accepted as root causes.

1. **Driver input current is incompatible with the multiplexer source impedance.** The magnitude of $I_B(R_S + R_{ON})$ is approximately 480 µV, and $I_B R_{FLAT(ON)}$ is approximately 72 µV. These values are consistent with S1 and S2 in magnitude. However, the submitted client brief says that S1 reads *low*, whereas the assumed ADA4807 current direction predicts a positive input-node shift. The magnitude diagnosis is high confidence; the polarity and measurement convention must be reconciled before the final root-cause statement is closed. Finding C-1.
2. **The reference sense point is before `R11`.** Any average REF current produces a sample-rate-dependent drop outside the feedback loop. Using the AD4002 datasheet value of 0.75 mA at 2 MS/s and a linear first-order model predicts about 231 ppm between 0.1 MS/s and 1.5 MS/s. The measured shift is only 90 – 100 ppm; therefore the mechanism is confirmed, but its exact magnitude is not yet reproduced. Finding M-1.
3. **The external input RC cannot settle a full-scale multiplexer step to half an 18-bit LSB within the 290 ns acquisition phase at 2 MS/s.** The first-order requirement is approximately 474 ns. A screening ceiling is therefore about 1.25 MS/s before amplifier and switch settling are added. This explains why S5 is signal dependent and why 1.5 MS/s is marginal, but the final product limit must be measured with the actual channel sequence. Finding M-3.

The powered-off hot-plug path is a genuine reliability gap. With only 100 Ω in series, a 4.2 V cell can force approximately 35 mA into the unpowered switch protection network, above the ADG1208 continuous S/D current rating. A fault-protected multiplexer is the preferred robust correction; simple silicon clamp diodes do not guarantee that current is kept out of the internal switch clamps. Finding C-2.

**Verdict on Q3.** The ±100 µV bench target is reachable only with a fixed calibration sample rate and a tighter reference grade. The recommended configuration uses a low-bias, fast JFET driver, an ADR4550D reference, a fault-protected multiplexer, corrected REF sensing, and a layout-controlled reference network. The conservative revised budget is ±88 µV at 23(3) °C and ±145 µV from 15 – 35 °C. Cross-rate accuracy and multiplexed high-speed operation remain validation items, not guaranteed outcomes.

| Where each client question is answered | | |
|---|---|---|
| Q1 | Error budget and S1–S3 mechanisms | §4, §5, §8 |
| Q2 | Rate dependence and the 2 MS/s question | §6 |
| Q3 | Reachability, minimal changes, and cost control | §1, §8, §10 |
| Q4 | Powered-off hot-plug mechanism and robust correction | §5 (C-2) |
| Q5 | Additional accuracy and robustness risks | §7 |

## 2 Object, Method, Severity, and Confidence

**Reviewed.** Schematic revision D, the client brief with symptoms S1–S7 and questions Q1–Q5, and current manufacturer documentation for every active device. PCB layout, firmware, production test software, and the future EIS module are out of scope. Findings that depend on placement or routing are explicitly marked as layout-critical.

**Method.** Error terms are derived symbolically and evaluated using the operating-condition tables that match this design. Typical values are used only to explain a measured typical effect; guaranteed limits are used when comparing the design against a hard specification. A mechanism is not called a complete root cause when sign, magnitude, or boundary conditions remain unresolved.

**Severity.** **Critical** prevents a stated target or creates a credible damage path. **Major** consumes a large share of the budget or creates a hidden operating dependency. **Minor** is a robustness, cost, or documentation issue.

**Confidence. High** means the schematic and datasheet arithmetic are sufficient. **Medium** means the mechanism is credible but requires a specified measurement. **Open** means an inconsistency must be resolved before the diagnosis is closed.

## 3 Findings Register

| ID | Severity | Finding | Confidence | Explains |
|---|---|---|---|---|
| C-1 | **Critical** | ADA4807 input current interacts with multiplexer $R_{ON}$ and flatness | Open sign / high magnitude | S1, S2, part S3 |
| C-2 | **Critical** | ADG1208 is exposed to powered-off cell injection | High | S7 |
| M-1 | **Major** | REF force point before `R11`; gain depends on throughput | Medium | S4 |
| M-2 | **Major** | REF capacitor loop is not controlled at the ADC pin | Medium / layout | risk |
| M-3 | **Major** | Input RC and channel settling limit multiplexed throughput | High for RC; medium system | S5 |
| M-4 | **Major** | ADR4550A tempco consumes the field budget | High | S3 |
| M-5 | **Major** | `C14` effective capacitance is unspecified at 5 V bias | High | risk |
| M-6 | **Major** | Present analog rail places the input near an amplifier input-pair transition | Medium | risk |
| N-1 | **Minor** | Precision grade of `R1`–`R8` has little value after C-1 | High | cost |
| N-2 | **Minor** | TVS/LDO coordination leaves little surge margin | High | robustness |
| N-3 | **Minor** | PTC choice is not coordinated with load and inrush | Medium | robustness |
| N-4 | **Minor** | `U8` dissipation and supply sequence are undocumented | Medium | robustness |

S6 is evidence, not a separate defect: averaging suppresses random noise but cannot remove deterministic transfer-function, drift, or reference-force errors.

## 4 Symptom-to-Root-Cause Map (Q1, Q2, Q4)

| Sympt. | Reported | Review conclusion | Status |
|---|---|---|---|
| S1 | Reads low by 430–520 µV | $\lvert I_B\rvert(R_S + R_{ON}) \approx 480\,\mu V$ matches magnitude, but the assumed current direction predicts the opposite polarity | polarity open |
| S2 | 60–85 µV bow after 2-point calibration | $\lvert I_B\rvert R_{FLAT(ON)} \approx 72\,\mu V$ is a strong quantitative match | high |
| S3 | 3.5–6 µV/°C | ADA4807 drift, $I_B/R_{ON}$ drift, and ADR4550A gain drift are all large enough; separate gain and offset vs. temperature | medium |
| S4 | 90–100 ppm shift, 0.1 to 1.5 MS/s | `R11` outside the sense loop necessarily creates the effect; datasheet-current model predicts 231 ppm, so exact magnitude requires measurement | medium |
| S5 | Several hundred µV at 2 MS/s | External RC requires 474 ns for $\pm 0.5\ \mathrm{LSB}_{18}$ vs. 290 ns acquisition; amplifier and MUX add further settling | high/medium |
| S6 | Averaging improves repeatability only | Consistent with deterministic dominant errors and the noise calculation in §9 | high |
| S7 | Stuck channel after powered-off hot-plug | Approx. 35 mA injection exceeds the ADG1208 continuous S/D current rating | high |

The review therefore closes S2, S6, and S7 at schematic level; identifies high- confidence contributors for S3 and S5; and leaves the S1 polarity and S4 exact magnitude as explicit validation questions.

## 5 Critical Findings

### C-1 Driver input bias current × multiplexer on-resistance CRITICAL

**Location.** `U5` (ADA4807-1) non-inverting input, fed from `U3` (ADG1208) through `R1`–`R8` (100 Ω).
**Mechanism.** In the relevant input common-mode region, the ADA4807 input current is approximately −1.2 µA typical. The ADG1208 single-supply table gives approximately 300 Ω typical on resistance and 60 Ω typical on-resistance flatness. Therefore

$$|\Delta V_{\text{level}}| \approx 1.2\,\mu\text{A}(100\,\Omega + 300\,\Omega) = 480\,\mu\text{V},$$
$$|\Delta V_{\text{bow}}| \approx 1.2\,\mu\text{A} \cdot 60\,\Omega = 72\,\mu\text{V}.$$

The second term is signal dependent and is not removed by a two-point calibration. It is comparable to, or larger than, the ADC's maximum INL of 3.2 LSB (approximately 61 µV).
**Polarity discrepancy.** With the stated current direction and a non-inverting follower, the source node moves positive. The client brief says the reported reading moves negative. Before release, confirm the error convention (DUT minus standard or standard minus DUT), the actual amplifier input polarity, and any digital sign or gain correction. This discrepancy does not invalidate the magnitude problem, but it prevents the phrase "complete root cause" from being used for S1.
**Recommendation.** Replace `U5` with a low-bias, fast JFET-input amplifier such as **ADA4625-1ARDZ**, subject to footprint and thermal review. Representative specifications are 15 pA typical input bias, 18 MHz GBW, and 48 V/µs slew rate. Its initial offset is removed by the existing two-point calibration; its offset drift must remain in the temperature budget. Raise the analog rail to approximately 9.5 – 10 V and verify input common-mode and output swing at all rail tolerances. Do not claim 2 MS/s multiplexed settling until V5 in §11 passes.

### C-2 Cell inputs are not protected when the board is unpowered CRITICAL

**Location.** `J2` pins 1–8 to the source pins of `U3`; only `R1`–`R8` are in series.
**Mechanism.** With `U3` unpowered, a connected cell can forward bias its internal protection network. A screening estimate is

$$I \approx \frac{4.2\,\text{V} - 0.7\,\text{V}}{100\,\Omega} \approx 35\,\text{mA},$$

which exceeds the ADG1208 continuous current rating for its analog terminals and can back-power the analog rail. The two returned units are therefore consistent with a credible design-induced failure mode.
**Recommendation.** Replace `U3` with a power-off/fault-protected multiplexer, preferably **ADG5208F**, which is specified for power-off protection and source overvoltage up to ±55 V. Its higher on resistance is acceptable after C-1 because the replacement driver's bias current is in the picoampere range. Confirm pinout/footprint, leakage over temperature, and the power-off current in V7. External BAV199 clamps are not the primary recommendation: their forward voltage does not guarantee that the internal ADG1208 clamps remain off, and they would inject current into an unpowered rail that has no defined sink.

## 6 Rate-Dependent Effects (Q2)

### M-1 Reference force point excludes R11 from the loop MAJOR

**Location.** `U4` feedback node versus `R11` (2.2 Ω) and the `C14`/REF node.
**Mechanism.** The ADC reference voltage is lower than the regulated buffer output by $I_{REF}R_{11}$. The AD4002 specifies 0.75 mA REF current at 2 MS/s. Under a linear first-order throughput model,

$$\Delta I_{REF}(0.1 \to 1.5\,\mathrm{MS/s}) \approx 0.525\,\mathrm{mA},$$
$$\Delta\varepsilon_{gain} \approx \frac{0.525\,\mathrm{mA}\cdot 2.2\,\Omega}{5\,\mathrm{V}} = 231\,\mathrm{ppm}.$$

The observed 90 – 100 ppm corresponds to an effective current change of only about 216 µA. This difference must not be hidden: it may reflect actual REF-current waveform, effective series resistance, buffer interaction, or the client's gain-measurement convention.
**Recommendation.** Sense the dc reference after `R11`, but treat this as a feedback-loop redesign rather than a wiring edit. Provide local ac feedback around `U4`, simulate the loop with the actual capacitor model, and verify with a load-step measurement. Until that passes, fix the sample rate as a calibration condition. Acceptance is defined by V4.

### M-2 Reference decoupling loop is not controlled at the REF pin MAJOR

The AD4002 requires a low-impedance reference source and local charge storage. A remote 10 µF capacitor can have sufficient capacitance but still present excessive ESL through its package and trace loop. The original 1.5 mV $Ldi/dt$ estimate was only an order-of-magnitude illustration, not a verified waveform prediction.
**Recommendation.** Place the main low-ESL reference capacitor directly at `U7` REF and GND pins, with the shortest possible loop. Select a part whose effective capacitance at 5 V bias is documented. Reserve a nearby 0402 pad for an optional 100 nF capacitor, but populate it only after an impedance or bench check confirms that the parallel network does not create an unacceptable anti-resonance. This finding is layout-critical.

### M-3 Input RC and channel settling versus rated conversion speed MAJOR

For `R12`=200 Ω and `C18`=180 pF, $\tau = 36$ ns. Settling a full-scale first-order step to ±0.5 LSB at 18 bits requires

$$t_{set} = \tau \ln(2^{19}) \approx 474\,\mathrm{ns}.$$

The AD4002 acquisition phase at 2 MS/s is 290 ns. Using the maximum 320 ns conversion time gives a screening throughput ceiling

$$f_{screen} \approx \frac{1}{320\,\mathrm{ns} + 474\,\mathrm{ns}} \approx 1.26\,\mathrm{MS/s},$$

before MUX transition, amplifier large-signal settling, ADC input kickback, and layout parasitics are added.
**Conclusion.** The ADC is rated for 2 MS/s; the submitted multiplexed source network is not automatically rated for an 18-bit full-scale channel step at that rate. Fixed-channel bursts may run faster than channel-to-channel scans. Define the product rate by the V5 first-conversion test and specify the number of discarded conversions after a channel change.

### Reference-buffer stability: not closed by schematic arithmetic

The isolation resistor and bulk capacitor are a reasonable starting topology, but a pole-zero estimate using an assumed open-loop output resistance is not a substitute for loop-gain data. The present configuration is assessed as *likely stable, bench verification required*. After moving the dc sense point, require a load-step response with monotonic settling or no more than one well-damped overshoot cycle, and no sustained ringing at any reference load or sample rate.

## 7 Accuracy Budget Consumers and Housekeeping

### M-4 Reference grade versus the field drift budget MAJOR

`U2` is ADR4550ARZ, specified at up to 4 ppm/°C. At full scale this is 20 µV/°C; relative to a 23 °C calibration, the worst field excursion to 35 °C is 240 µV. The reference alone can therefore consume essentially the complete ±250 µV requirement.

**Recommendation.** Use **ADR4550D** (maximum 0.8 ppm/°C, specified from 0 – 70 °C) if its LCC package is acceptable. The product's 15 – 35 °C field range is inside that grade's specified range. ADR4550B is acceptable for wider ambient coverage, but its 2 ppm/°C limit leaves only about 3 µV of conservative bench margin when combined with ADC INL and other reserves.

### M-5 C14 dc-bias derating is unspecified MAJOR

A generic 10 µF, 10 V, 0805 X7R capacitor cannot be assumed to retain 10 µF at 5 V. The reduction depends on manufacturer, case size, dielectric formulation, temperature, and lot.

**Recommendation.** Specify a 16 – 25 V 1206/1210 part with a manufacturer dc-bias curve and require at least 5 µF effective capacitance at 5 V across the production temperature range. Record the effective design value in the BOM, not only the nameplate value.

### M-6 Analog-rail headroom and amplifier input transition MAJOR

The present approximately 7 V rail places a 5 V input close to the ADA4807 input-stage transition region where bias current and offset behavior change. The original report treated the transition as a hard common-mode limit; it is more accurately an error-discontinuity risk.

**Recommendation.** With the proposed ADA4625-1, set the analog rail to approximately 9.5 – 10 V, then verify input common-mode range, output swing, dissipation, and regulator tolerance using the selected orderable part. The divider value must be recalculated from the actual ADP7118 configuration; no resistor value is approved by this schematic-only review.

### Minor findings

| | |
|---|---|
| **N-1** | After C-1, the 0.1 %/25 ppm/K grade of `R1–R8` has negligible influence on dc accuracy. Retain thin-film construction for leakage and voltage-coefficient control, but 1 % tolerance is adequate. |
| **N-2** | ADP7118 is specified for operation to 20 V; its absolute maximum VIN is 24 V. A nominally 24 V TVS clamp therefore does not provide useful operating margin and may exceed the absolute maximum at surge current and tolerance. Coordinate TVS, source impedance, input capacitor, and a polymer damping capacitor by transient test. |
| **N-3** | The 0.25 A PTC protects only against gross faults, but a 50 mA replacement must not be selected without checking cold resistance, hot-plug inrush, hold current at temperature, and trip energy. Record the coordination calculation. |
| **N-4** | Feeding the 1.8 V regulator directly from 12 V is thermally inefficient but low risk at the stated load. Verify startup ordering against the AD4002 requirements and record the result in the production test specification. |

# 8 Consolidated Error Budget (Q1, Q3)

## 8.1 Conservative dc limits after two-point calibration

The table below uses arithmetic addition for hard specification comparison. The as-designed column uses the observed upper bow for C-1 because a guaranteed maximum for the combined $I_B R_{FLAT}$ mechanism is not available from the submitted data. The revised column uses maximum or reserved limits. Sample rate is fixed to the calibration rate; cross-rate transfer is reported separately.

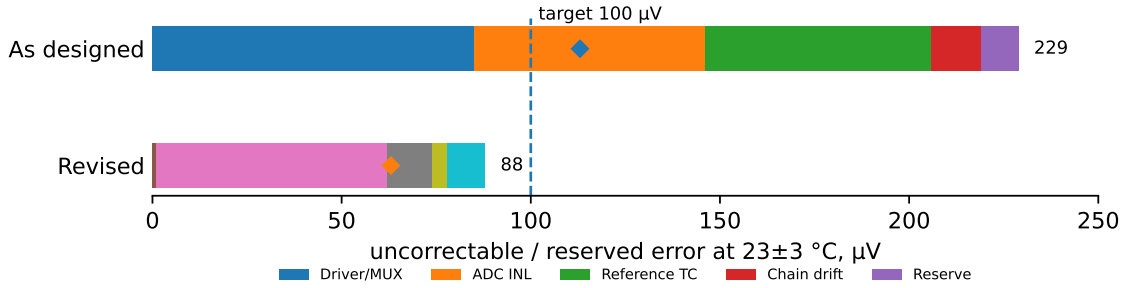
| | As designed | | Revised | |
|---|---|---|---|---|
| Term (µV) | 23 ± 3 °C | 15–35 °C | 23 ± 3 °C | 15–35 °C |
| Driver/MUX residual nonlinearity | 85 | 85 | 1 | 1 |
| ADC INL, maximum | 61 | 61 | 61 | 61 |
| Reference tempco (A / D grade) | 60 | 240 | 12 | 48 |
| Driver and chain drift | 13 | 54 | 4 | 15 |
| Metrology, thermal-EMF, and unmodelled reserve | 10 | 20 | 10 | 20 |
| **Conservative sum, fixed rate** | **229** | **460** | **88** | **145** |
| **Target** | 100 | 250 | 100 | 250 |
| **Margin** | −129 | −210 | +12 | +105 |

## 8.2 Expected-performance screening

For engineering yield estimation only, independent typical terms may be combined by RSS. This is not a substitute for the conservative limit above.

| | 23 ± 3 °C | 15–35 °C |
|---|---|---|
| As-designed RSS estimate | 113 µV | 265 µV |
| Revised RSS estimate | 63 µV | 82 µV |

The rate-dependent term is excluded because calibration is specified at a fixed rate. In the present design, S4 adds a measured 450 – 500 µV full-scale-equivalent error when moving from 100 kS/s to 1.5 MS/s. The revised acceptance target is no more than 10 ppm (50 µV at full scale) across the explicitly supported rates.




Conservative error stack at 23 ± 3 °C; diamonds mark RSS screening estimates.

# 9 Noise and Operating Rate

## 9.1 As-designed noise budget

Using the submitted 4.42 MHz input pole (ENBW $= \frac{\pi}{2} f_c = 6.95$ MHz), the approximate per-conversion input-referred noise is:

| Source | rms per conversion |
|---|---|
| ADA4807 voltage noise | 8.2 µV |
| Johnson noise, approximately 400 Ω | 6.8 µV |
| Amplifier current noise through source impedance | 0.7 µV |
| AD4002 total rms noise, datasheet | 30.4 µV |
| **RSS total** | **32.2 µV** |
| After ideal 64-sample average | 4.0 µV |

This is consistent with S6: the repeatability target can be met while the mean result remains wrong because the dominant defects are deterministic.

### 9.2 Revised driver and scan-rate implications

ADA4625-1 has approximately the same wideband voltage-noise class as ADA4807, so the averaged noise target remains feasible. The replacement does not, however, create an automatic 2 MS/s multiplexed signal chain. Large-signal slew, 18-bit settling, the external RC, switch transition, and ADC kickback must be tested together.

Recommended operating model:

- For precision logging, use a fixed channel or channel burst, discard the characterized number of conversions after each MUX transition, and calibrate at the production sample rate.
- Treat 1 MS/s as a validation point, not a guaranteed specification. Attempt 2 MS/s only on a fixed channel or after V5 proves the required settling margin.
- Keep the averaging window asynchronous to any amplifier chopping or periodic digital activity, and verify spectral spurs rather than assuming $1/\sqrt{N}$ behavior indefinitely.

## 10 Change List (deliverable 2)

| Refdes | Now | Change to / action | Finding |
|---|---|---|---|
| `U5` | ADA4807-1AKSZ | ADA4625-1ARDZ; verify footprint, exposed pad, common mode, and stability | C-1 |
| `U3` | ADG1208 | ADG5208F; verify pinout/footprint and leakage | C-2 |
| `U4` feedback | before `R11` | dc sense after `R11`; add local ac feedback only after loop analysis | M-1 |
| `U7 REF` | remote `C14` | move qualified low-ESL bulk capacitor to REF/GND pins; reserve optional 0402 pad | M-2 |
| `U2` | ADR4550ARZ | ADR4550D grade; LCC footprint change | M-4 |
| `C14` | 10 µF/10 V/0805 | 10 µF/16 – 25 V, 1206/1210, $C_{eff} \geq 5$ µF at 5 V | M-5 |
| Analog rail | approx. 7 V | recalculate for 9.5 – 10 V; verify LDO loss and tolerances | M-6 |
| `R1–R8` | 0.1 % | 1 % thin film, leakage-clean layout | N-1 |
| Input supply | ceramic only | add damped bulk capacitance after transient analysis | N-2 |
| `F1` | PTC 0.25 A | select from coordinated hold/trip/inrush calculation | N-3 |

A preliminary distributor-price comparison places the net BOM change in the order of $7–$9 per unit, but this is not a quotation. Purchasing must confirm orderable grades, package availability, and volume price before the $10 constraint is declared met.

## 11 Validation Plan

The revised design is accepted only by the following measurements. The dc source and DMM uncertainty must be stated in the test record; “10 microvolt class” is not a sufficient metrology specification.

| ID | Measurement | Acceptance |
|---|---|---|
| V0 | Confirm error definition, amplifier input polarity, and raw code sign using a 1 mV positive input step | S1 sign convention documented; predicted and observed polarity agree |
| V1 | Raw and calibrated error at 0.5 V, 2.5 V, and 4.5 V, all channels | raw offset documented; calibrated midpoint error $\leq 20\,\mu V$ excluding ADC INL sweep |
| V2 | 33-point sweep 0.25 – 4.75 V after two-point calibration | $\lvert\text{residual}\rvert \leq 80\,\mu V$; no repeatable bow above 20 µV after subtracting ADC INL estimate |
| V3 | Chamber 15 – 35 °C; fit offset and gain separately using at least two input levels | gain slope $\leq 1.2\,\text{ppm}/^\circ\text{C}$; offset slope $\leq 1.5\,\mu V/^\circ\text{C}$ |
| V4 | Calibrate at 100 kS/s; measure fixed-channel gain at 0.4, 1.0, and 1.5 MS/s where supported | $\lvert\Delta gain\rvert \leq 10\,\text{ppm}$; REF pin and buffer output recorded simultaneously |
| V5 | Alternate adjacent channels at 0.2 V and 4.8 V; measure each conversion after MUX change versus rate | identify discard count $N$; first accepted conversion $\leq 1\,\text{LSB}_{18}$ error at each specified rate |
| V6 | 10 000 conversions with input shorted at the connector | $\leq 45\,\mu V$ rms raw; $\leq 7\,\mu V$ after 64-sample average |
| V7 | Board unpowered: apply 4.2 V and harness transients to each channel, then repeat V1/V2 | source current within ADG5208F power-off specification; no rail back-powering and no parametric shift |
| V8 | Reference-buffer load step and impedance check with final capacitor population | stable, well-damped settling; no sustained ringing or anti-resonant peak that violates V4/V5 |

A focused revision check of the corrected schematic should be completed before layout release. PCB review remains necessary for M-2, C-2 creepage/current paths, guarding, thermal gradients, and thermoelectric junction placement.

## 12 Assumptions and Data Sources

| Item | Basis / sensitivity |
|---|---|
| AD4002 REF current | 0.75 mA at 2 MS/s, 5 V REF; linear throughput scaling is a first-order assumption and is explicitly tested by V4 |
| AD4002 timing | 290 ns acquisition phase and 270 – 320 ns conversion time at rated conditions |
| ADA4807 / ADG1208 interaction | typical 1.2 µA input current, 300 Ω on resistance, and 60 Ω flatness; used to explain typical magnitude, not a guaranteed production maximum |
| ADG1208 hot-plug screen | Approximate 0.7 V internal clamp drop; actual current sharing is device- and transient-dependent |
| ADR4550 temperature term | Full-scale input-referred gain error; calibration temperature 23 °C, worst field excursion 12 °C |
| Revised driver drift | ADA4625-1 maximum offset-drift allowance rounded into the conservative chain term; production test confirms actual behavior |
| Metrology reserve | Explicit placeholder for calibration-source uncertainty, DMM transfer uncertainty, thermal EMF, and unmodelled PCB leakage; replace with a formal uncertainty budget before release |

Manufacturer documents used: ADG1208/ADG1209 Rev. E; ADA4807 Rev. B; AD4002/AD4006/AD4010

Rev. A; ADR45xx Rev. G; ADP7118 Rev. H; ADA4625-1 Rev. B; ADG5208F Rev. B. Orderable part numbers and revisions must be rechecked at procurement release.

## 13 Scope, Limitations, and Clarification

This review covers schematic revision D only. It does not replace SPICE/driver tool analysis, PCB review, prototype validation, or a calibrated measurement uncertainty analysis. Statements labelled medium or open are hypotheses with a defined closure test, not final facts. The revised conservative budget is valid only for a fixed calibration sample rate and the stated 15 – 35 °C product range.

### Clarification round (recorded)

**Client.** Can we keep the ADA4807 and remove its error in software?

**HighSNR.** A single offset coefficient is insufficient. The $R_{ON}$-flatness term varies with signal level, and the input-stage behavior also varies with common mode and temperature. A dense per-channel map could reduce it, but that conflicts with the stated production calibration. Replacing the driver is the lower-risk correction.

**Client.** Why not retain the eight BAV199 clamps?

**HighSNR.** Because their forward voltage does not guarantee priority over the multiplexer internal clamps, and the upper diode would inject current into an unpowered rail. A power-off-protected multiplexer defines the fault state at component level and is easier to validate.

**Client.** Does the revised circuit support 2 MS/s?

**HighSNR.** The ADC supports the rate; the multiplexed chain is not approved at 2 MS/s. Fixed-channel bursts may pass, but channel switching requires V5 and a documented discard count.