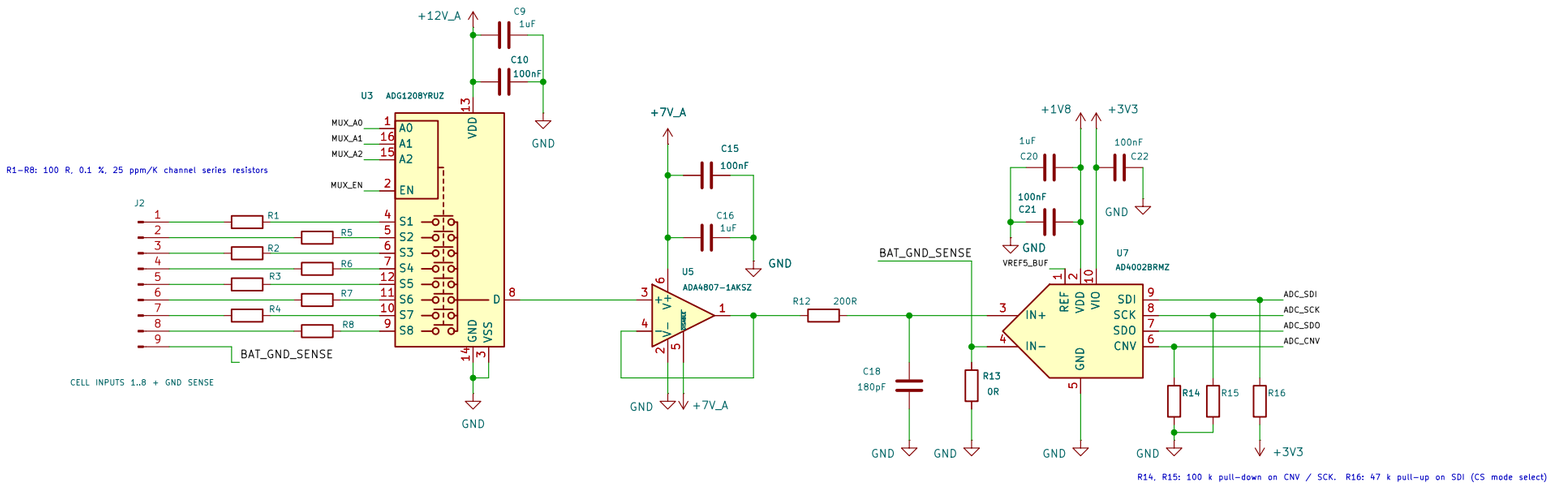
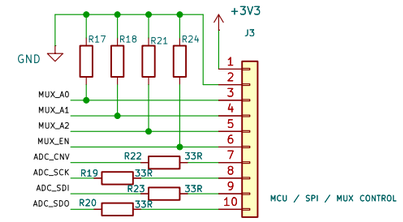
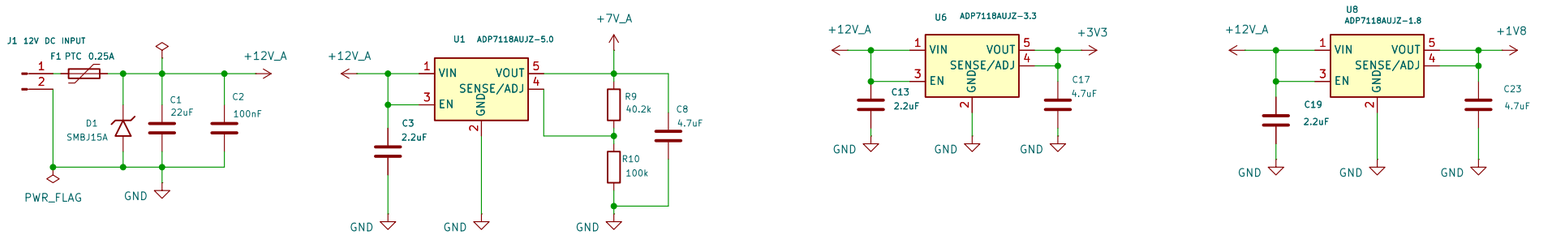
1. CELL INPUTS / MULTIPLEXER / ADC



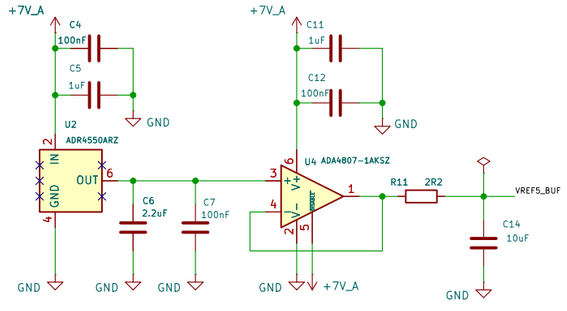
2. MCU CONTROL / SPI TERMINATION



3. INPUT PROTECTION / POWER RAILS



4. PRECISION 5 V REFERENCE



DESIGN NOTES

1. Battery topology: eight independent cells sharing one negative terminal at J2.9. Series-stack operation is not supported by this front end.
2. Cell input range 0 ... 5.000 V referred to J2.9. No input attenuation is fitted.
3. J2.9 is a sense-only return. Load current must not be routed through this conductor.
4. J3.1 is a +3V3 OUTPUT, 20 mA maximum, for logic-level interfacing only.
5. Analog rail +7V_A = 7.01 V nominal, set by R9 / R10 on the SENSE/ADJ pin of U1.
6. R13 is the single-point link between the battery sense return and analog ground.
7. All electrolytic-free: ceramic dielectrics only. See BOM fields for voltage rating and dielectric class of every capacitor.

REVISION HISTORY

A	2026-05-18	Concept study, single-channel breadboard equivalent
B	2026-06-24	Reference buffer added, supply rails split into three regulators
C	2026-07-22	Multiplexer package selection, sheet annotation pass
D	2026-07-23	Library alignment (project symbols), BOM fields normalised, ERC clean, net names corrected, D1 changed to unidirectional TVS

EIS excitation / load subsystem is a separate assembly, out of scope for this sheet.
Symbols: project library HighSNR.kicad_sym. ERC clean, no unconnected pins.
Topology: 8 independent cells, common negative return at J2.9. Series stack NOT supported.
AD4002 18-bit 2 MSPS pseudo-differential SAR; 8-channel multiplexed dc front end

HighSNR Lab

Sheet: /
File: battery_tester_rev_c.kicad_sch

Title: 8-Channel Precision Battery Cell Voltage Acquisition Front-End

Size: A3	Date: 2026-07-23	**Rev: D**
KiCad E.D.A. 10.0.0		Id: 1/1