Client Brief — Design Review Request

8-Channel Precision Battery Cell Voltage Acquisition Front-End

Project: 8-Channel Precision Battery Cell Voltage Acquisition Front-End
Schematic under review: `battery_tester_rev_d.kicad_sch` (rev D, 2026-07-23)
Engagement: Extended schematic review, fixed fee $2,300 per quote SNR-Q-2607
Client: Celladyne Instruments (name changed; brief published with the client's permission as a worked example)

---

1. Who we are and what we are building

We are a six-person team building a desktop battery cell characterization instrument: eight independent cell fixtures, per-channel electronic load, and a shared precision voltage acquisition front end — the subject of this review. Our background is embedded systems and power electronics; we do not have a dedicated precision-analog specialist on staff.

The acquisition front end must log open-circuit and under-load cell voltage for eight **independent** cells (each fixture has its own negative lead brought back to the sense connector). A separate EIS excitation/load module is planned for next year; this front end should not preclude it, but EIS is otherwise out of scope.

Accuracy targets (after a two-point calibration at 23 °C, per channel):

Condition	Target
23 ± 3 °C (bench)	± 100 μV
15…35 °C (field)	± 250 μV
Resolution / repeatability	≤ 20 μV rms after averaging

We selected an 18-bit SAR ADC (AD4002), a 5 V precision reference (ADR4550) and what we understood to be an appropriate driver amplifier based on the ADC vendor's application material. On paper the component specs exceed our targets by a wide margin. The hardware does not.

2. History and current status

- **Rev A** (May 2026): single-channel concept board. Looked fine at the resolution we could measure then.
- **Rev B** (June 2026): full 8-channel board, three supply rails, buffered reference. This is the hardware all measurements below come from.
- **Rev C / Rev D** (July 2026): multiplexer package correction and library/BOM cleanup only — **no electrical changes to the signal path**. Rev D is what we are submitting for review, ahead of the next layout.

Five rev B units exist. We have a calibrated 6.5-digit DMM (Keysight 34465A), a small thermal chamber, and a fixed-point voltage source good to about 10 μV for checks.

3. What we measure on rev B

Numbered so the review can reference them directly.

S1 — Large raw offset, same sign on every channel.
Before calibration every channel reads low by 430–520 μV depending on the unit. It calibrates out, but nothing in our error budget predicted an offset of this size, and we would like to know where it comes from before we trust the rest of the budget.

S2 — Residual bow after calibration.
After two-point calibration (0.5 V and 4.5 V points) a sweep against the DMM shows a smooth, roughly parabolic residual of 60–85 μV peaking around mid-scale. It is stable and repeats across units. The ADC is specified at $\pm$3.2 LSB INL ($\sim$61 μV), so we assumed this is simply the ADC — but the shape and consistency across five units makes us doubt that.

S3 — Temperature drift far above budget.
In the chamber, calibrated readings walk 3.5–6 μV/°C between 15 and 35 °C. Over the field range that alone is 70–120 μV, most of our $\pm$250 μV budget. The reference is specified at 4 ppm/°C (20 μV/°C referred to 5 V), so the reference cannot explain all of it, and we have not identified the rest.

S4 — Calibration does not transfer across sample rate.
We normally log at $\sim$100 kSPS bursts, but during bring-up for the future EIS mode we ran the converter near 1.5 MSPS. Gain shifted by roughly 90–100 ppm ($\sim$0.5 mV at full scale) relative to the 100 kSPS calibration — repeatably, in the same direction, on every unit. Recalibrating at the new rate fixes it, but we do not understand the mechanism, and a calibration that silently depends on sample rate worries us.

S5 — Performance collapse at the ADC's rated 2 MSPS.
At the full 2 MSPS the errors become signal-dependent and grow into the several-hundred-μV range. We currently cap at $\sim$1.5 MSPS and things are "mostly fine", but the datasheet says 2 MSPS and we would like to know whether the limitation is our board or our expectations.

S6 — Averaging fixes repeatability but nothing else.
Averaging 64 samples brings repeatability comfortably under 10 μV rms, but S2, S3 and S4 are completely unaffected. So whatever these are, they are not noise, and adding more averaging or a better reference low-pass (both of which we tried) is money spent in the wrong place.

S7 — Two field failures after harness hot-plug.
Two evaluation units came back with single stuck channels (3 on one unit, 7 on the other) reading near full scale. Both users admit connecting cell harnesses while the instrument was unpowered or off. Nothing else on the boards was damaged. We would like to know whether this is coincidence or a design gap.

4. What we already tried / ruled out

- Swapped the ADC and the reference IC between a "good" and "bad" unit — symptoms stayed with the board, not the parts.
- Re-flowed grounding around the connector area; no change.
- Replaced the reference bulk capacitor with a larger one; no change to S2–S4.
- Reviewed our own schematic twice internally. It passes ERC and matches the vendor's reference

signal chain part-for-part, which is exactly why we are stuck: we cannot see anything wrong, yet the numbers say otherwise.

5. Questions we are paying to have answered

1. Build the actual dc error budget of this signal chain as designed — where do S1, S2 and S3 come from, term by term, with numbers?
2. Explain the sample-rate dependence (S4) and the 2 MSPS behavior (S5). Is 2 MSPS achievable with this topology at all?
3. Is the $\pm 100\ \mu$V / $\pm 250\ \mu$V target reachable with this architecture and a comparable BOM cost, or do we need a different approach? If reachable — the minimal set of changes, prioritized.
4. Assess S7: is there a plausible damage mechanism in the current input circuit, and what is the cheapest robust fix that does not compromise accuracy?
5. Anything else in the schematic that will bite us at these accuracy levels — including things we did not think to ask about.

6. Constraints

- Next layout starts in three weeks; we can absorb component and minor circuit changes, not a full re-architecture, unless the review shows the architecture itself is the problem (see Q3 — we want a straight answer either way).
- BOM delta preferably under $10 per unit.
- No per-unit oven calibration in production; a single-temperature two-point calibration is what manufacturing has signed up for.
- Eight independent cells with a common sense return is a fixed interface decision for this generation; series-stack support is explicitly not required.

7. Deliverables agreed for the $2,300 fee

1. Written review report: quantified error budget, root cause for each symptom S1–S7, prioritized change list with part numbers.
2. Marked-up schematic or change table referenced to our reference designators.
3. One follow-up call (up to 90 minutes) with our team after we read the report.

We are deliberately not sharing our internal guesses about root causes beyond what is written above, so the review starts from the schematic and the measured behavior, not from our assumptions.

— R. T., Engineering Lead, Celladyne Instruments